Course Code	Course Name	Credit
CSC304	Digital Logic & Computer Organization and Architecture	3

Pre-requisite: Knowledge on number systems	
Course Objective:	
1	To have the rough understanding of the basic structure and operation of basic digital circuits and digital computer.
2	To discuss in detail arithmetic operations in digital system.
3	To discuss generation of control signals and different ways of communication with I/O devices.
4	To study the hierarchical memory and principles of advanced computing.
Course Outcome:	
1	To learn different number systems and basic structure of computer system.
2	To demonstrate the arithmetic algorithms.
3	To understand the basic concepts of digital components and processor organization.
4	To understand the generation of control signals of computer.
5	To demonstrate the memory organization.
6	To describe the concepts of parallel processing and different Buses.

Module		Detailed Content	Hours
1		**Computer Fundamentals**	**5**
	1.1	Introduction to Number System and Codes	
	1.2	Number Systems: Binary, Octal, Decimal, Hexadecimal,	
	1.3	Codes: Grey, BCD, Excess-3, ASCII, Boolean Algebra.	
	1.4	Logic Gates: AND, OR, NOT, NAND, NOR, EX-OR	
	1.5	Overview of computer organization and architecture.	
	1.6	Basic Organization of Computer and Block Level functional Units, Von-Neumann Model.	
2		**Data Representation and Arithmetic algorithms**	**8**
	2.1	Binary Arithmetic: Addition, Subtraction, Multiplication, Division using Sign Magnitude, 1's and 2's compliment, BCD and Hex Arithmetic Operation.	
	2.2	Booths Multiplication Algorithm, Restoring and Non-restoring Division Algorithm.	
	2.3	IEEE-754 Floating point Representation.	
3		**Processor Organization and Architecture**	**6**
	3.1	Introduction: Half adder, Full adder, MUX, DMUX, Encoder, Decoder(IC level).	
	3.2	Introduction to Flip Flop: SR, JK, D, T (Truth table).	
	3.3	Register Organization, Instruction Formats, Addressing modes, Instruction Cycle, Interpretation and sequencing.	
4		**Control Unit Design**	**6**
	4.1	Hardwired Control Unit: State Table Method, Delay Element Methods.	
	4.2	Microprogrammed Control Unit: Micro Instruction-Format, Sequencing and execution, Micro operations, Examples of microprograms.	
5		**Memory Organization**	**6**
	5.1	Introduction and characteristics of memory, Types of RAM and ROM, Memory Hierarchy, 2-level Memory Characteristic,	
	5.2	Cache Memory: Concept, locality of reference, Design problems based on	

		mapping techniques, Cache coherence and write policies. Interleaved and Associative Memory.	
6		**Principles of Advanced Processor and Buses**	**8**
	6.1	Basic Pipelined Data path and control, data dependencies, data hazards, branch hazards, delayed branch, and branch prediction, Performance measures-CPI, Speedup, Efficiency, throughput, Amdhal's law.	
	6.2	Flynn's Classification, Introduction to multicore architecture.	
	6.3	Introduction to buses: ISA, PCI, USB. Bus Contention and Arbitration.	

Textbooks:	
1	R. P. Jain, "Modern Digital Electronic", McGraw-Hill Publication, 4thEdition.
2	William Stalling, "Computer Organization and Architecture: Designing and Performance", Pearson Publication 10TH Edition.
3	John P Hayes, "Computer Architecture and Organization", McGraw-Hill Publication, 3RD Edition.
4	Dr. M. Usha and T. S. Shrikanth, "Computer system Architecture and Organization", Wiley publication.
References:	
1	Andrew S. Tanenbaum, "Structured Computer Organization", Pearson Publication.
2	B. Govindarajalu, "Computer Architecture and Organization", McGraw-Hill Publication.
3	Malvino, "Digital computer Electronics", McGraw-Hill Publication, 3rdEdition.
4	Smruti Ranjan Sarangi, "Computer Organization and Architecture", McGraw-Hill Publication.

Assessment:	
Internal Assessment:	
Assessment consists of two class tests of 20 marks each. The first class test is to be conducted when approx. 40% syllabus is completed and second class test when additional 40% syllabus is completed. Duration of each test shall be one hour.	
End Semester Theory Examination:	
1	Question paper will comprise of 6 questions, each carrying 20 marks.
2	The students need to solve total 4 questions.
3	Question No.1 will be compulsory and based on entire syllabus.
4	Remaining question (Q.2 to Q.6) will be selected from all the modules.

Useful Links	
1	https://www.classcentral.com/course/swayam-computer-organization-and-architecture-a-pedagogical-aspect-9824
2	https://nptel.ac.in/courses/106/103/106103068/
3	https://www.coursera.org/learn/comparch
4	https://www.edx.org/learn/computer-architecture